Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of synchronizing one or more devices on a first bus, the first bus associated with a first clock for generating first bus timing information for the first bus with one or more devices on a second bus, the second bus associated with a second clock for generating second bus timing information for the second bus, each of the devices having an individually adjustable timing, the method comprising:

acquiring the first bus timing information and the second bus timing information from the first bus and the second bus respectively;

determining a timing offset between the first bus and the second bus; and,

broadcasting the timing offset to the one or more devices on the second bus; and,

adjusting the timing of the one or more devices on the second bus to be synchronized with the one or more devices on the first bus based upon the broadcast timing offset and the second bus timing information wherein the one or more devices on the second bus comprise cameras and the cameras

adjust their timing by selectively reading an adjustable amount of extra data from a light-sensing array for each frame.

2. (Cancelled)

3. (Previously Presented) A method according to claim 1 comprising calculating a drift rate of the timing offset and broadcasting the drift rate to the one or more devices on the second bus and adjusting the timing of the one or more devices on the second bus to be synchronized with the one or more devices on the first bus based on the timing offset and the drift rate and the second bus timing information.

4. (Previously Presented) A method according to claim 3 wherein calculating the drift rate comprises calculating a first order time derivative of the timing offset.

5. (Withdrawn - Previously Presented) A method according to claim 4 wherein calculating the drift rate comprises calculating a second order time derivative of the timing offset.

6. (Original) A method according to claim 1 wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on timing information of the first bus.

7. (Original) A method according to claim 6 wherein the one or more devices on the second bus adjust their timing by determining timing information of the first bus by applying the timing offset to the timing information of the second bus.

8. (Withdrawn) A method according to claim 1 wherein the one or more devices on the second bus adjust their timing by adjustably controlling a delay to alter a length of an operational cycle.

9. (Cancelled)

10. (Withdrawn) A method according to claim 1 wherein the first and second buses comprise serial buses.

11. (Withdrawn) A method according to claim 1 wherein the first and second buses comprise USB buses.

12. (Cancelled)

13. (Withdrawn) A method according to claim 1 wherein the first and second buses comprise different types of buses.

14. (Cancelled)

15. (Previously Presented) A method according to claim 1 comprising automatically broadcasting timing information on the first and second buses.

16. (Previously Presented) A method according to claim 1 wherein the method is carried out on a data processor comprising first and second interfaces coupled to the first and second buses, respectively, and wherein acquiring timing information from the first bus and the second bus comprises querying the first and second interfaces for the timing information.

17. (Withdrawn - Previously Presented) A method according to claim 1 wherein broadcasting the timing offset to the one or more devices on the second bus is carried out on a synchronization unit coupled between the first and second

buses, and wherein acquiring timing information from the first bus and the second bus comprises receiving timing information from the first and second clocks at the synchronization unit.

18. (Cancelled)

19. (Currently Amended) A method of synchronizing one or more devices on a first bus, the first bus associated with a first clock for generating first bus timing information for the first bus with one or more devices on a second bus, the second bus associated with a second clock for generating second bus timing information for the second bus, each of the devices having an individually adjustable timing, the method comprising:

providing a master bus on which a global time is broadcast by a master clock;

acquiring the first bus timing information and the second bus timing information from the first bus and the second bus respectively;

determining a first timing offset between the first bus and the master bus;

determining a second timing offset between the second bus and the master bus; and,

broadcasting the first timing offset to the one or more devices on the first bus and broadcasting the second timing offset to the one or more devices on the second bus; and,

adjusting the timing of the one or more devices on the first bus based upon the first timing offset and the first bus timing information and adjusting the timing of the one or more devices on the second bus based upon the second timing offset and the second bus timing information so that the one or more devices on the first bus and the one or more devices on the second bus all begin their respective operational cycles at the same global time wherein the one or more devices on the second bus comprise cameras and the cameras adjust their timing by selectively reading an adjustable amount of extra data from a light-sensing array for each frame.

20. (Original) A method according to claim 19 wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on the global time.

21. (Cancelled)

22. (Currently Amended) An apparatus for synchronizing one or more devices on a first bus, the first bus associated with a first clock for generating first bus timing information for the first bus with one or more devices on a second bus, the second bus associated with a second clock for generating second bus timing information for the second bus, each of the devices having an individually adjustable timing, the apparatus comprising:

a first interface coupled to the first bus;

a second interface coupled to the second bus;

a processing element coupled to the first and second buses by the first and second interfaces respectively to receive the timing information for the first and second buses;

a program memory coupled to the processing element, the program memory containing software instructions programmed to cause the processing element to calculate a timing offset between the first bus and the second bus and broadcast the timing offset to the one or more devices on the second bus by means of the second interface; and,

a timing control system in each of the one or more devices on the second bus, the timing control systems each configured to adjust a timing of a corresponding one of the devices based upon the second bus timing information and the timing offset wherein the one or more devices on the second bus comprise cameras and the cameras adjust their timing by selectively reading an adjustable amount of extra data from a light-sensing array for each frame.

23. (Original) An apparatus according to claim 22 wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on timing information of the first bus.

24. (Original) An apparatus according to claim 23 wherein the one or more devices on the second bus are configured to adjust their timing by determining timing information of the first bus by applying the timing offset to the timing information of the second bus.

25. (Original) An apparatus according to claim 22 wherein a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus

exceeds a maximum allowable bandwidth of either of the first or second buses.

26. (Original) An apparatus according to claim 22 wherein the first and second interfaces, the processing element and the program memory are all located within a data processor configured to process data received from the one or more devices on the first bus and the one or more devices on the second bus.

27. (Withdrawn - Previously Presented) An apparatus according to claim 22 wherein the first interface, the processing element and the program memory are all located within a first data processor configured to process data received from the one or more devices on the first bus and the second interface is located within a second data processor configured to process data received from the one or more devices on the second bus, and wherein the first and second data processors are connected by a network connection.

28. (Withdrawn) An apparatus according to claim 22 wherein the first and second interfaces, the processing element and the

program memory are all located within a synchronization unit coupled between the first and second buses.

29. (Currently Amended) An apparatus according to claim 22 wherein the one or more devices on the first bus comprise a first plurality of cameras, and the one or more ~~devices~~ cameras on the second bus comprise a second plurality of cameras, and wherein all of the first and second pluralities of cameras are positioned to ~~encircle an image area and to~~ record images of ~~the~~ an image area.

30. (Previously Presented) A method according to claim 1 comprising simultaneously broadcasting the timing offset to a plurality of devices on the second bus and individually regulating a timing of each of the plurality of devices on the second bus based at least in part upon the timing offset.

31. (Previously Presented) A method according to claim 19 comprising simultaneously broadcasting the timing offset to a plurality of devices on the second bus and regulating a timing of each of the plurality of devices on the second bus based at least in part upon the timing offset.

32. (Previously Presented) An apparatus according to claim 22 comprising a plurality of devices on the second bus wherein each of the devices on the second bus is configured to regulate its timing based at least in part upon the timing offset and timing information from the second bus.